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ALTERNATIVE TO PTO/SB/08a/b (06-03)

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known Application Number Not yet assigned 10/1537124 Filing Date June 2, 2005 First Named Inventor Sachin AGGARWAL Art Unit Not yet assigned 2823 Examiner Name Not yet assigned B. KEBEDE	
Sheet	1	of	1	Attorney Docket Number 492322028400	

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
BK	1.	6,552,402-B1	4-22-2003	Ozasa et al.	_____

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
BK	2.	JP-08-274259	10-18-1996		abstract
	3.	JP-2000-036582	2-2-2000		abstract
	4.	JP-2000-091504	3-31-2000		abstract
BK	5.	JP-2001-168197	6-22-2001		abstract

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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
BK	6.	Mao-Feng et al. (2001) "Current Mirror Layout Strategies for Enhancing Matching Performance," Analog Integrated Circuits and Signal Processing 28, pp. 9-26			
BK	7.	Marcel J. M. Pelgrom et al. (1989) "Matching Properties of MOS Transistors," IEEE Journal of Solid-State Circuits 24(5), pp. 1433-1439			

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Examiner Signature	/Brook Kebede/	Date Considered	02/28/2007
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